What is Claimed is:

1. A packet processing circuit comprising:

a plurality of macros each of which processes packet data on the basis of a clock and outputs the processed packet data from at least one route, said macros being cascade-connected; and

a clock supply unit which supplies the clock to a macro to be controlled and, when no packet data is output for a predetermined time from all routes of a macro on an input side of said macro to be controlled, stops supplying the clock to said macro to be controlled.

2. A circuit according to claim 1, wherein said clock supply unit comprises

a clock buffer which supplies the clock to said macro to be controlled, and

a clock management unit which causes said clock buffer corresponding to said macro to be controlled to stop supplying the clock when no packet data is output for the predetermined time from all the routes of said macro on the input side of said macro to be controlled.

3. A circuit according to claim 2, wherein

said macro on the input side comprises a first

signal output unit which outputs, to said clock management unit, a first packet output notification signal which indicates that the packet data is output, and

said clock management unit comprises a packet output detection unit which causes said clock buffer to start supplying the clock when the first packet output notification signal is enabled and stop supplying the clock when the first packet output notification signal is not enabled again within the predetermined time.

4. A circuit according to claim 3, wherein said packet output detection unit comprises a counter circuit which detects the predetermined time by counting the number of clocks, said counter circuit resetting a count value when the first packet output notification signal is turned on.

5. A circuit according to claim 4, wherein said counter circuit detects the predetermined time by counting the number of clocks necessary until the packet data passes through said macro on the input side.

6. A circuit according to claim 3, wherein

said macro on the input side comprises a plurality of routes to output the processed packet data, and

said first signal output unit outputs, to said clock management unit, a first packet output notification signal which indicates that the packet data is output from at least one of the routes.

7. A circuit according to claim 6, wherein said macro on the input side comprises a second signal output unit which outputs, to said first signal output unit for each of the routes, a second packet output notification signal which indicates that the packet data is output, and

said first signal output unit comprises a gate circuit which generates the first packet output notification signal by ORing the received second packet output notification signal.